(a) Exemplary claim 4 includes:

"inverter means ... operative to provide a sinusoidal AC voltage between a first and a second AC terminal; the inverter means being operative for a part of each fundamental period to cause the first AC terminal to be at the same potential as that of the first DC terminal; the part having a duration approximately one quarter that of the fundamental period".

This feature is neither disclosed nor suggested by Zansky '600.

In Zansky '600 (Fig. 2), a sinusoidal voltage is provided between terminals 45 and 46. However, neither one of these terminals is caused, during each cycle of the AC voltage, "to be at the same potential as that of the first DC terminal" for a duration equal to one quarter of the total duration of each cycle.

In particular, the potential at Zansky's terminal 46 is never equal to that of either of the DC terminals, while the potential at his terminal 45 varies in a sinusoidal manner and is at most equal to the B+ (or B-) voltage for a vanishingly brief period once or twice each cycle and not for anything near a quarter of the duration of that cycle.

If Examiner were to maintain his position to the contrary, he is asked to show exactly where Zansky identifies two AC terminals across which there is a sinusoidal voltage while, at the same time, the potential of one of these terminals is caused "to be at the same potential as that of" one of the DC terminals for a duration equal to one quarter of the total duration of each cycle.

Examiner rejected claims 8, 13, 18 and 24 under 35 USC 102b as being anticipated by Zansky '087.

Applicant accepts the rejection of claim 13; which has been amended to obviate Zansky '087 as a reference.

However, Applicant traverses Examiner's rejection of claims 8, 18 and 24 for the following reasons.

(b) In effect, exemplary claim 8 defines a reference terminal and a first and second AC terminals across which is a sinusoidal AC voltage; yet, at the same time, the voltage between the reference terminal and the first AC terminal is non-sinusoidal; and so is the voltage present between the reference terminal and the second AC terminal.

Thus, at the first and second AC terminal exist two non-sinusoidal voltages which, in differential combination, yield a sinusoidal voltage.

This feature is neither disclosed nor suggested in Zansky '087.

For an illustration of the subject matter defined by exemplary claim 8, Applicant refers to waveforms (h) and (i) of Fig. 14, neither of which waveforms is sinusoidal -- or, conversely, both of which waveforms are non-sinusoidal. Yet, the differential combination of these two non-sinusoidal waveforms yields a sinusoidal waveform, as illustrated by waveform (j) of Fig. 14.

If Examiner were to persist in his position to the effect that the subject matter of exemplary claim 8 is disclosed in Zansky '087, Applicant requests of Examiner to identify two terminals in Zansky '087 that would correspond to Applicant's first and second AC terminals.

(c) Dependent claim 24 (now independent claim 39) defines an arrangement that has a "first means" wherein:

"(i) the first means includes an inverter having a first and second ... transistor means; (ii) a first transformer means is connected with control terminals of the first transistor means, which first transformer means has a first ferro-magnetic core ...; (iii) a second transformer means is connected with control terminals of the secod transistor means, which second transformer means has a second ferro-magnetic core ...; and (iv) the first ferro-magnetic core is magnetically separate from the second ferro-magnetic core".

This feature is neither disclosed nor suggested in Zansky '087.

If Examiner were to persist in a position to the contrary, Applicant requests of Examiner to show eaxactly where in Zansky '087 this feature is disclosed. More particularly, Examiner is asked to identify in Zansky '087 the equivalents of Applicant's first and second ferro-magnetic cores.

Re Amended Claim 13

Amended claim 13 includes:

"a source providing a DC voltage ... the source being connected with the power line voltage ... the power line voltage having a peak magnitude; the magnitude of the DC voltage being substantially higher than the peak magnitude".

This feature reflects the arrangement illustrated by Applicant's Fig. 2.

In Fig. 2, when ordinary 120Volt/60Hz power line voltage is provided between terminals 33 and 37, the magnitude of the DC voltage resulting between DC terminals 39 and 38 is twice the peak magnitude of the power line voltage.

The arrangement of Fig. 2 has a priority date going back at least to 08/14/80; which is the filing date of Applicant's Serial No. 06/178,107, now abandoned.

Examiner rejected claims 10, 12, 20 and 22 under 35 USC 112, second paragraph, as being indefinite.

Applicant traverses these rejections for the following reasons.

(d) With respect to a given reference terminal, junction Jx is substantially at the same potential as is junction Jq. This is so for the reason that transformers ST1 and ST2 are saturable current transformers with a primary-to-secondary step-up turns ratio higher than 3:1; which means that the magnitude of any voltage present across each primary winding is only a small fraction of one Volt; which is magnitude quite negligible in comparison with the magnitude of the voltage provided from the ballast output terminals Jx and Jy.

Re Allowed Claims 14-17, 19, 21, 23 and 25-28

These claims, which all depended from claim 13, have now been written in independent form as claims 29-32, 34, 36 and 39-43, respectively.

Re New Claims

New claims 44-54 are all readable on the circuit arrangements illustrated by Applicant's Figs. 2 through 8; the subject matter of which circuit arrangements has a priority date no later than 08/14/80. In fact, the subject matter of most of new claims 44-54 has a priority date going back to 03/20/78.

Thus, the Zansky references are not applicable prior art with respect to new claims 44-54.

IN THE DRAWINGS

Corrected drawings have been ordered and will be provided in response to the next office action.